Effectiveness of PCB Perimeter Via Fencing

Radially Propagating EMC Emissions Reduction Technique

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***Abstract* – Via fencing around the periphery of a printed circuit board is a practice to attempt to eliminate radially propagated energy from the edge of a board. This study comparatively analyzed via fenced boards against unfenced boards as well as investigated other emission related design variables including trace distance from the PCB edge, termination loads, and via fence spacing. The S_{21} measurements were taken with a network analyzer and a horn antenna with the PCB trace as the source. Frequency sweeps from 1-8.5GHz showed that via fencing attenuated as much as 21dB at some frequencies, concluding that via fencing was definitively beneficial. Trace distances to the edge of the board showed mixed results at lower frequencies, but gave higher emissions with smaller distances to the edge at higher frequencies. Varying loads yielded results showing emissions for given loads were highly dependent on frequency with the exception of the dominant short-circuit load. Via fence spacing was shown to be significant, but only loosely followed the 1/8th wavelength rule of thumb. This study proved to be very important for the electronics industry as EMC regulations are increasingly harder to meet with shrinking die process technologies and rising clock frequencies.**

***Keywords* – Printed circuit board, via fencing, radial propagating emissions.**

I. Introduction

One of the dominant mechanisms [1] of emissions is radially propagated electromagnetic waves excited by currents through vias and traces which are funneled by pseudo-waveguides by the top and bottom layer ground and/or power planes. Most of the energy is transmitted into air from the PCB's edge causing EMC radiated emissions as shown in Fig. 1. The frequencies of the radiated energy are dependent on the via heights (PCB thickness) and trace lengths, and amplitudes change with the distance through the dielectric and its properties. Other variables, such as substrates (dielectrics), will not be examined in this study.

To combat this problem some designers have used the 20-H Rule which is a practice of recessing one plane by a distance of twenty times the distance between the two parallel planes. This practice has been studied and shown to only minimally reduce emissions [2] and in some cases, such as a 2 layer stack-up, the emissions were increased [3] due to the recessed plane allowing the opposite plane to become a patch antenna – transferring the emissions from the X and Y axis to the Z axis.

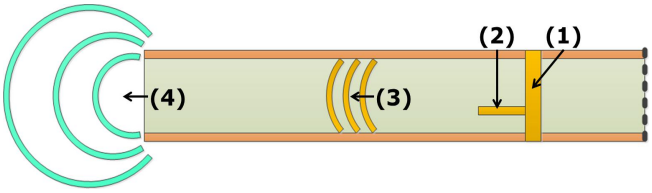

Fig. 1. Sources including (1) vias and (2) internal asymmetric stripline traces. Ground planes are effective waveguide for (3) incident wave and the (4) transmitted wave.

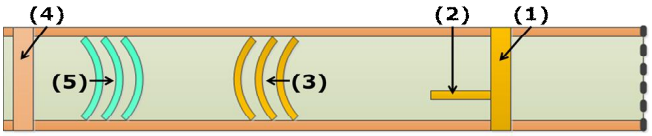

Fig. 2. Cross-sectional view of the via fencing theory: Sources including (1) vias and (2) internal asymmetric stripline trace and ground planes as waveguide for (3) incident wave as before, but (4) ground stitching vias creates an impedance boundary that (5) reflects the wave internally.

This also removes valuable layout real estate which makes the practice inefficient and ineffective.

One concept that is more practical in current designs is utilizing impedance boundaries as an advantage, illustrated by Figure 2. The goal of minimizing transmitted energy is achieved by maximizing reflected energy. A normal PCB provides what is effectively an infinite (open) impedance boundary. Knowing that with open impedance boundaries energy can be measured coming from the edge of the PCB, other impedance boundary values should be investigated.

The top and bottom ground planes in the Z direction and the perimeter ground terminations in the X and Y directions create a three dimensional zero-impedance boundary. This theoretically keeps the energy internal to the PCB structure since it is reflected from the perimeter keeping it from being emitted. This can be done with edge plating or via fencing, but edge plating has many negative side-effects [4] including the need for unmasked copper bands around the perimeter of both planes for the plating to connect to, the inability for 100% coverage due to handling needs during manufacturing, and only selective chemical nickel-gold finishes suitable as choices.

There have been multiple studies and reports about the general subject of via fencing but their work is limited to analyzing the via itself as the source of radiation [1] and via fencing being used to minimize crosstalk [5] between signals internal to the design.

The rule of thumb that a stub starts to become reactive as it approached 1/8th of a wavelength has been known and followed since the early 70's [5]. This same principle shows that the space between vias also starts to look reactive as the spacing approaches 1/8th of a wavelength. That supposedly means that if the spacing between ground fencing vias is less than 1/8th of a wavelength, via fencing should appear to be the same as a solid ground impedance barrier. To utilize the 1/8th wavelength principle for this study, the well-known frequency-to-wavelength equation was altered slightly to reflect the 1/8th wavelength as shown in Eq. 1.

$$Via\ Spacing \leq \frac{\lambda}{8} = \frac{8C_0}{f\sqrt{\varepsilon_r}} \quad (1)$$

The relationship of frequency to wavelength – and with Eq. 1 also via fencing – is shown in Table I. According to this 1/8th wavelength rule, for an emission regulation ceiling of 2 GHz, via spacing of about 375 mils should be enough to suppress the radiation of any frequencies of interest.

TABLE I. RELATION BETWEEN WAVELENGTH AND VIA SPACING

Spacing (mils)	λ (in)	Frequency (GHz)
25	0.20	30.274
50	0.40	15.137
100	0.80	7.568
150	1.20	5.046
200	1.60	3.784
300	2.40	2.523
500	4.00	1.514
1000	8.00	0.757

This study was intended to determine whether perimeter via fencing for reducing EMC emissions is effective when compared to adequate ground paths through vias for sub-10GHz frequencies. To expand on this subject, this paper will also address other potential questions regarding via fencing and PCB design. While identifying the variables involved that might have effect on radially propagating emissions, it was discovered that this study could address multiple aspects of PCB design. The derived secondary purposes of the study encompassed the effects of parallel distance from a signal trace to the edge of the board, varying termination loads, and if the 1/8th wavelength rule of thumb correctly estimates via fencing spacing.

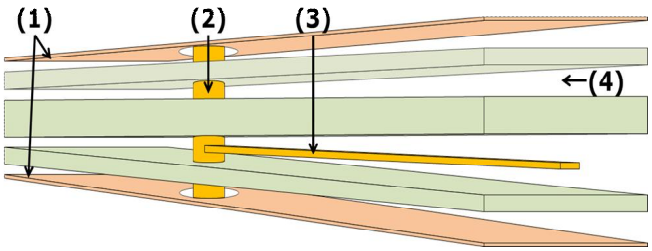

Fig. 3. Expanded view of the study's PCB design and antenna: (1) Top and bottom conductor layers as ground planes. (2) Vias used to connect trace antenna to load/coaxial header. (3) Internal conductor layer 3 with a trace used as an antenna. (4) Notice conductor layer 2 is missing.

II. METHODS

Prototype Fabrication

The PCB design was intended to emulate industry electronic design practices as closely as possible to make the value higher for current electronic and PCB design. For this reason FR408 material was chosen as the dielectric material and 1 ounce copper layers with silver finish. The board outline was chosen to be 4 inches by 4 inches due to panelizing reasons and to increase the ease of handling. All vias were a common 15 mil drill hole with 1 mil plating.

A 3 layer PCB was designed using the external conductive layers used as the ground planes and a single trace on the internal layer serves as the sourcing antenna as shown in Figure 3. This resulting asymmetric stack-up was chosen to emulate normal 4-layer PCB manufacturing practices.

The antenna length was chosen to be 2.15 inches, being an approximate resonant length for 5.49 GHz, which is at the high end for DDR DQ and other high speed transmission lines lengths and well within the 1-8.5 GHz capability of the VNA used for this study.

. Using a Saturn PCB Design Tool [7], the trace width to obtain 50Ω characteristic impedance was 13 mils when using the asymmetrical stripline parameters and the FR408 relative permittivity of 3.8. A standard 62 mil board thickness meant the height from the layer 3 trace to the bottom layer is 9.45 mils, and the distance from the top conductive layer is 49 mils.

To make sure the different designs can be objectively compared, both the fenced and the unfenced boards were designed to have identical numbers of vias. This, in theory, created the same number of paths to ground and avoided contamination of the study by eliminating any unwanted variables. For a similar reason, all eight of the PCB designs were made into one panel to avoid any potential plating differences between fabrication runs.

Study Variables Addressed

To address the study's first and main facet of whether via fencing helps when compared to unfenced boards, there were two major layout topologies. Four of the boards had perimeter via fencing and four had vias only on the two sides that are perpendicular to the trace antenna and have no bearing on the

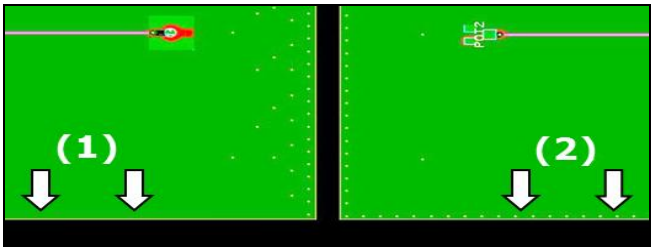

Fig. 4. An unfenced board (1) next to a fenced board (2).

direction of interest. Fig. 3 shows how the vias are oriented with a fenced board vs. an unfenced board.

The second aspect of the PCB design addressed the trace distance from the edge of the board. To achieve this, half of the boards had the trace positioned 0.25 inches from the edge of the board while the other half had the trace at a distance of 1.5 inches. Each of the boards had the ability to yield two measurements by rotating the board 180°, as Fig. 5 shows.

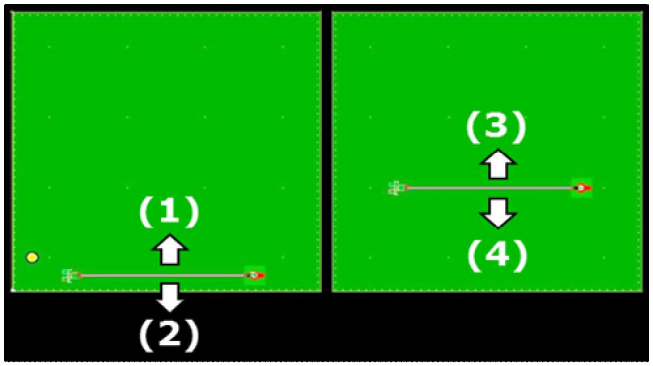

Fig. 5. Trace antenna placements yielding set-ups of (1) 3.75", (2) 0.25", (3) 2.5", and (4) 1.5" distances to the edge of the PCB.

The next design parameter was the terminating load on the trace. SMT 0805 and 1206 1% tolerance resistors were used. Both the MCX co-axial connector and the resistors were designed as surface mount parts to make sure there were no undesired frequency components due to through-holes. The first value chosen as a load was 47.5Ω. Next was the open load followed by the shorted to represent a capacitive load. The shorted load was achieved by using 0Ω jumper resistors. The last load to be tested was a 10kΩ load. This was desired because of its selection as a common value in industry as a pull-down with many IC pins need to be pulled to a desired low state or to give voltages a path to ground for dissipation.

The final design characteristic was the via spacing itself. Since this study analyzed frequencies in the single digit GHz, Fig. 6 shows the spacing of 100 mils and 150 mils chosen. This, in theory, should create a pseudo-high pass filter for emitted energy. Recalling the previously discussed relationship between frequency and via spacing, 100 mil spacing should have a corner frequency of 7.6 GHz and 150 mil spacing results in a corner frequency of 5.0 GHz. As the spacing increased in the via fencing on the layout, more vias had to be moved to the edges perpendicular to the trace, but as mentioned above the number of vias was kept the same.

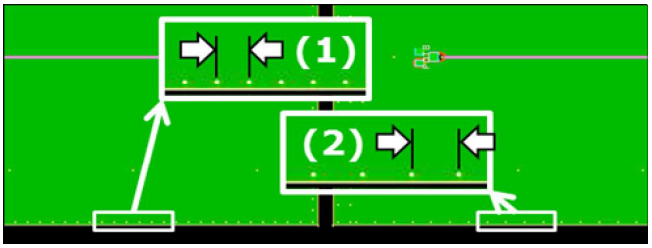

Fig. 6. Different via fence spacing of 100 mils (1) and 150 mils (2) should give different emissions cut-off frequencies.

Experiment Set-Up

The test set-up itself was with a horn antenna as the receiver, the PCB as the emitting structure, and the network analyzer as the source. The horn antenna was placed in the horizontal direction inline and at the same height as the PCB as shown in Fig. 7 to measure the radially propagating waves emitting from the edge of the boards.

The distance from the receptor of the horn to the close edge of the PCB was measured at 22.75 cm for all measurements taken. It was placed fairly close to the PCB to ensure that the measurements were as definitive as possible. Initial measurements were taken at varying distances showing that the horn placement had a linear relationship, and a closer position merely yielded higher magnitudes.

The board outline was marked on the foam structure shown in Fig. 8 used to elevate the PCB to ensure repeatability between measurements. An Agilent Technologies E5071C ENA Series network analyzer was used and performed a

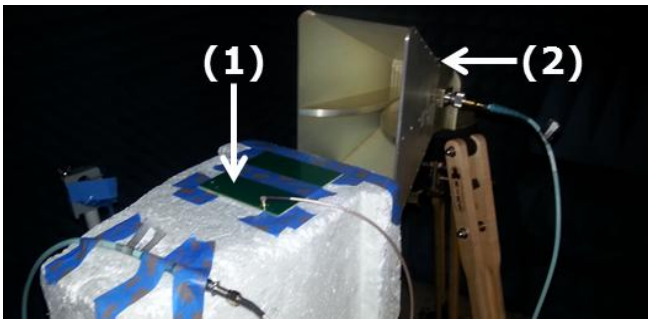

Fig. 7. View of the test setup including PCB (1) as the emitting structure sourced by the network analyzer and the horn antenna (2) as the receiver.

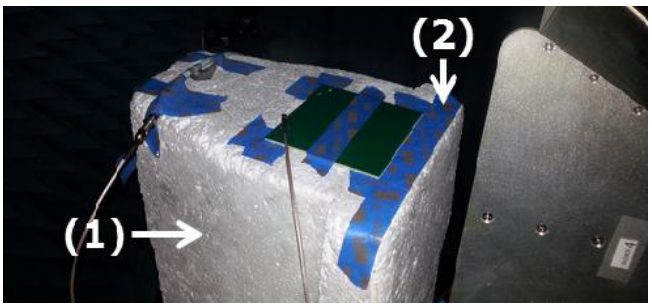

Fig. 8. View of the foam test stand (1) and the alignment markings (2) for repeatability.

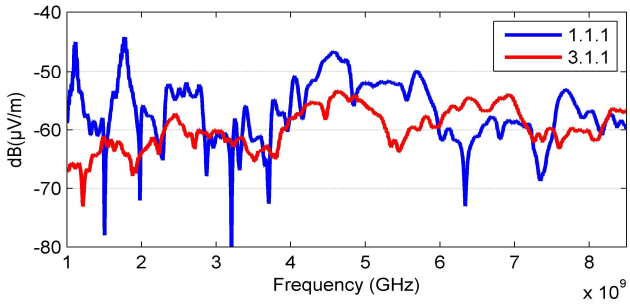

Fig. 9. The significant difference between non-via fenced (1.1.1) vs. via fenced (3.1.1) with 0.25" trace spacing and 50 Ω load.

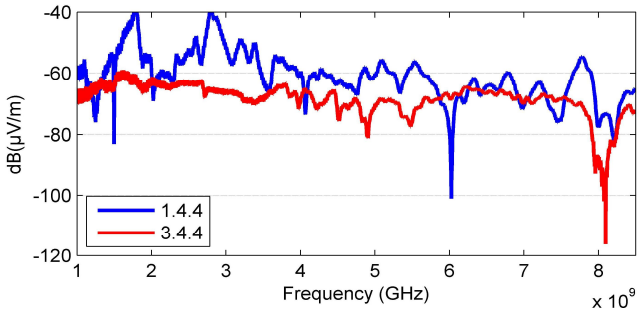

Fig. 10. Another example of emissions for fenced (3.4.4) compared to unfenced (1.4.4) with 3.75" trace spacing and 10 kΩ load.

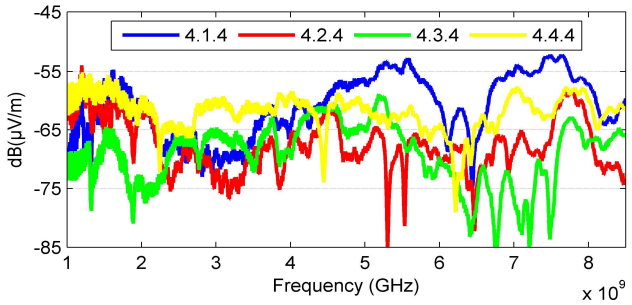

Fig. 11. Varying trace distances of 0.25" (4.1.4), 1.5" (4.2.4), 2.5" (4.3.4), and 3.75" (4.4.4) with an unfenced PCB and 10 kΩ load yielded unusual results until midway through the frequency spectrum scanned.

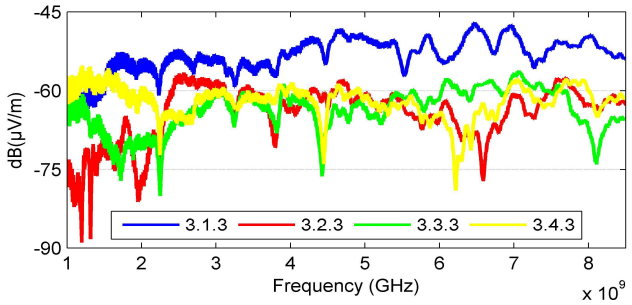

Fig. 12. Varying trace distances of 0.25 inches (3.1.3), 1.5 inches (3.2.3), 2.5 inches (3.3.3), and 3.75 inches (3.4.3) with 100 mil fenced PCB and shorted load show another example of having an expected outcome only at higher frequencies.

frequency sweep of 1-8.5 GHz and recorded each S_{21} measurement.

To ease the potential confusion with the 64 permutations, a simple indexing convention was created and shown below in Table II. The first term of the name is which board style it is. The second term is the antenna distance to the edge of the board. The last term is the load.

TABLE II. NAMING INDEX KEY: "BOARD . DISTANCE . LOAD"

Board Key		Distance Key		Load Key	
1	Unfenced 100 mil spacing	1	0.25"	1	50
2	Unfenced 150 mil spacing	2	3.75"	2	Short
3	Fenced 100 mil spacing	3	1.5"	3	Open
4	Fenced 150 mil spacing	4	2.5"	4	10k

III. RESULTS

The effectiveness of perimeter via fencing was well emphasized across the study. As seen in Fig. 9 with 0.25 inch trace distance to the PCB edge and a 50 Ω load, the via fenced PCB emitted less energy than the open-ended PCB's almost across the frequency range. Differences of 21.56 dB at 1.11 GHz and 20.34 dB at 1.78 GHz were the largest observed. From 1.00 GHz to 2.80 GHz the average attenuation of the fenced PCB's was 7.35 dB less, which is a significant improvement. Fig. 10 shows another example of a non-fenced board emitting much more energy than a fenced board.

The trace distance from the edge of the PCB did have an effect on emissions. At some frequency ranges the trace with the greatest distance from the edge of the board actually emitted the highest energy. Fig. 11 shows this from 1.99 GHz to 3.24 GHz with a maximum difference of 7.41 dB and averaged 3.84 dB more energy emitted than any other distance. Fig. 11 also shows frequency ranges where the expected result of the smallest distance to the PCB's edge had the highest emissions, as is such from 4.31 GHz to 6.38 GHz and again from 6.51 GHz to the end of the measured spectrum.

Measurements taken with a shorted load and the 100 mil via fence spacing in Fig. 12 below shows more examples where frequencies between 1.00 GHz and 1.51 GHz the trace farthest from the edge of the PCB radiated the highest electrical field. However, between frequencies of 2.85 GHz and 6.03 GHz it did not appear to matter how far from the edge the trace is as long as it is more than a half an inch or so. For the previous range mentioned the measured E field difference between the 1.5 inch, 2.5 inch, and 3.75 inch trace distances averages only 3.3 dB maximum difference. This including the large dips for the 2.5 inch and 3.75 inch trace distances where the maximum difference peaks at 14.1 dB.

There was a significant variance across the study based on the terminating loads. As Fig. 13 shows, the predominant emitter was the shorted load. With a 150 mil via fence and a 2.5 inch distance from the trace to the edge of the board, the only frequencies where the shorted load was not dominant

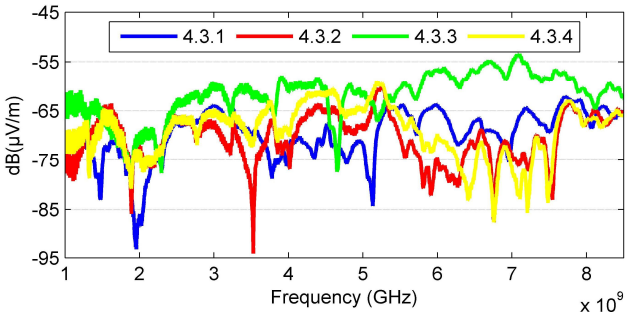

Fig. 13. Varying loads of 50Ω (4.3.1), open (4.3.2), short (4.3.3), and 10kΩ (4.3.4) with a 150 mil fenced board and 2.5" trace distance.

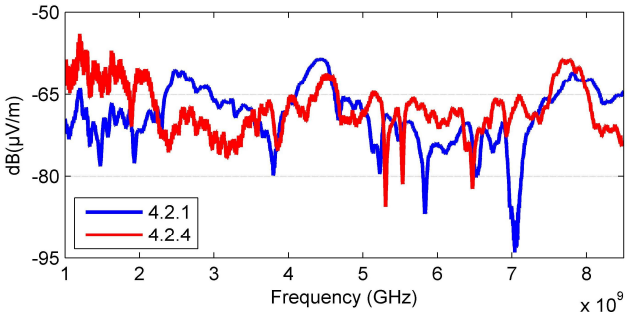

Fig. 14. Resistive load compare of 50 Ω (blue) and 10 kΩ (red) terminations with a 150 mil fenced board and 1.5" trace distance.

were the small frequency ranges of 1.48 GHz to 2.00 GHz, from 4.51 GHz to 4.72 GHz, and again from 5.06 GHz to 5.31GHz. The open load had a maximum margin of 17.23 dB at 6.98 GHz which is a very high difference. It was noted that the 50 Ω load did not have the least emissions across the tested spectrum as hypothesized. It was the lowest for certain ranges as shown from 1.24 GHz to 2.66 GHz and again from 3.70 GHz to 5.33 GHz with the exception of the two valleys that briefly intersect; the shorted load at 4.03 GHz and the open load at 4.65 GHz.

There was a switching of dominance of emissions between the 50 Ω load and the 10 kΩ loads when directly compared in Fig. 14. From 1.00 GHz to 2.22 GHz the 10 kΩ load emitted on average 8.31 dB more than the 50 Ω load; which is what was hypothesized. Unexpectedly, the two cross and exchange places and up to 3.53 GHz the 50 Ω load emits on average 6.55 dB more. For the rest of the frequencies the 10 kΩ load edges the 50 Ω load for emissions by a small 1.54 dB margin on average, but with difference as high as 26.73 dB at 7.06 GHz.

The results for varying via spacing in Fig. 15 showed the 100 mil spaced fencing and the 150 mil spaced fencing measurements were virtual copies of each other until the 4.20 GHz mark, where up to that point they averaged a difference of only 1.36 dB. After around 4.6 GHz the emissions for the two fenced boards are continuously dissimilar from each other. The 150 mil spaced board had a calculated corner frequency of 5.05 GHz, but even beyond 7 GHz the unfenced board and the 150 mil fenced boards measure quite different magnitudes. The one exception is from 7.58 GHz to 7.71 GHz where the measured values of all three boards were within 5 dB.

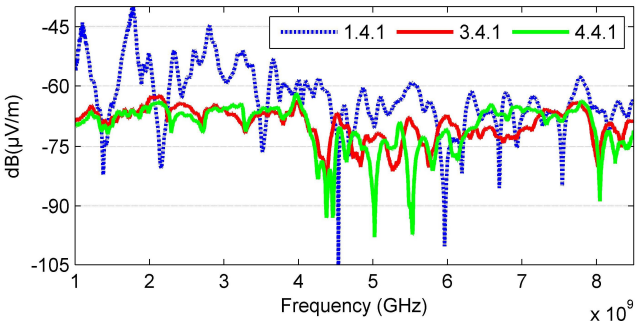

Fig. 15. The 1/8th wavelength rule was tested by comparing the unfenced (1.4.1) against 100 mil spaced (3.4.1) and 150 mil spaced via fencing (4.4.1) with 3.75" trace distance and 50 Ω load configuration.

IV. Discussion

The effectiveness of perimeter via fencing for radially propagating emissions was evident in the study. The benefit of via fenced PCB's when compared to the unfenced PCB's with respect to emissions was reinforced in every direct comparative measurement at a majority of frequencies, albeit not uniformly across all frequencies and configurations. A secondary observation when measuring via fenced boards was that fencing seemed to stabilize the peaks and valleys in some places, however again, not across all frequencies and configurations. The measurements on fenced boards had much smaller ΔdB and lessened the more drastic slopes and changes of electric field magnitudes across frequencies than the open-ended boards.

The trace distance from the edge of the PCB did have an effect on emissions, but not consistently in the way hypothesized in the introduction of this study. There was an unexpected result of the trace farthest from the board edge emitted more than any other trace at some lower frequencies, but for the most part the trace spaced only a quarter of an inch from the edge dominated the emissions as expected. These mixed results means that a design rule for whether or not via fencing should be used cannot be based on trace distance from the edge of the PCB alone.

Varying loads yielded different results for emissions. At specific frequencies the difference in magnitude was negligible for all load/trace distance/board style configurations, but in some cases it mattered greatly. The short circuit had the highest emissions over most of the frequency ranges which is what many capacitive loads would look like at these higher frequencies. The open circuit load emulated something like a test point and had the least emissions about half the time. When the 50Ω load was directly compared to the 10kΩ load there was a switching of dominance between 1GHz to 3.5GHz that is attributed to the internal resonance due to the PCB dimensions. This goes to show – like the varying trace distance compare – a design rule for whether or not via fencing should be used cannot be based on what termination load is used alone.

Spacing between the vias of perimeter fencing did have a small amount of influence on the measured emissions, but for

this study the results were less than conclusive. Neither of the two boards emulated the reference unfenced board and continued to attenuate emissions well past the calculated frequency using the 1/8th wavelength rule. The plots did seem to converge relative to the unfenced board, but there was enough difference to doubt the effectiveness of the 1/8th wavelength rule of thumb for via spacing.

This study used very carefully controlled variables in a minimally populated board and layout. It should be noted that a full electronics design will have multiple sources with multiple loads and a vast difference in trace distances from the edges of the board.

A real-world design will also have a number of vias already in the design by necessity. Via fencing will add to the number in the design, not just be repositioned. Additional vias are not usually an adder for unit cost as the set-up is what is time consuming. Going from 1,000 vias to 2,000 will only add a couple pennies on even moderately low annual unit volumes.

Via fencing as a practice could have some potential negative side-effects to signal integrity since the energy does have to couple to something. There could also be some concern to introducing some internal resonance issues, and both of these concerns should be noted when attempting to put via fencing into practice for PCB design.

There are also some possible ramifications to perimeter vias for manufacturing purposes, such as potential for accidental grounding of a metal enclosure. This would cause a lack of case isolation – and creating a possible antenna for a vehicle level EMC emission source – if a unit is so designed.

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